

	L #	Hits	Search Text	DBs
1	L1	4180	(sequenc\$3 issu\$3 dispatch\$3) near10 instruction near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
2	L2	455796	(status state condition) near10 (network rout\$3 bus connect\$3 interconnect\$3 path line)	USPAT; US-PGPUB
3	L3	7078	2 near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
4	L4	522	1 and 3	USPAT; US-PGPUB
5	L5	35351	((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem)).ab,ti.	USPAT; US-PGPUB
6	L6	287	4 and 5	USPAT; US-PGPUB
7	L7	594	(sequenc\$3 issu\$3 dispatch\$3) near10 instruction near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	EPO; JPO; DERWENT; IBM_TDB
8	L8	277642	(status state condition) near10 (network rout\$3 bus connect\$3 interconnect\$3 path line)	EPO; JPO; DERWENT; IBM_TDB
9	L9	2470	8 near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	EPO; JPO; DERWENT; IBM_TDB
10	L11	15	7 and 9	EPO; JPO; DERWENT; IBM_TDB

	Docum ent ID	U	Title	Current OR
1	US 51215 02 A	<input type="checkbox"/>	System for selectively communicating instructions from memory locations simultaneously or from the same memory locations sequentially to plurality of processing	712/24
2	US 51214 88 A	<input type="checkbox"/>	Sequence controller of an instruction processing unit for placing said unit in a ready, go, hold, or cancel state	712/229
3	US 51094 95 A	<input checked="" type="checkbox"/>	Method and apparatus using a source operand list and a source operand pointer queue between the execution unit and the instruction decoding and operand processing units of a pipelined data processor	712/207
4	US 50776 63 A	<input checked="" type="checkbox"/>	Information processing system having microprogram-controlled type arithmetic processing unit with information transfer through a system control unit upon fault detection	714/10
5	US 50670 69 A	<input checked="" type="checkbox"/>	Control of multiple functional units with parallel operation in a microcoded execution unit	712/218
6	US 50582 03 A	<input checked="" type="checkbox"/>	Mobile telephone terminal having selectively used processor unit for low power consumption	455/574
7	US 50560 15 A	<input checked="" type="checkbox"/>	Architectures for serial or parallel loading of writable control store	703/27
8	US 50401 08 A	<input checked="" type="checkbox"/>	Information processing system having microprogram-controlled type arithmetic processing unit with clock synchronization instruction	709/400
9	US 50383 12 A	<input checked="" type="checkbox"/>	Data processing system capable of performing vector/matrix processing and arithmetic processing unit incorporated therein	708/520
10	US 50364 54 A	<input checked="" type="checkbox"/>	Horizontal computer having register multiconnect for execution of a loop with overlapped code	712/241
11	US 50290 74 A	<input checked="" type="checkbox"/>	Bus adapter unit for digital processing system	710/306
12	US 50219 45 A	<input checked="" type="checkbox"/>	Parallel processor system for processing natural concurrencies and method therefor	712/216
13	US 50199 66 A	<input checked="" type="checkbox"/>	Dual processors using busy signal for controlling transfer for predetermined length data when receiving processor is processing previously received data	710/29
14	US 49947 24 A	<input checked="" type="checkbox"/>	Servo-controlled automatic door having automatic detecting and adjusting mechanism	318/603
15	US 49929 33 A	<input checked="" type="checkbox"/>	SIMD array processor with global instruction control and reprogrammable instruction decoders	712/22
16	US 49911 23 A	<input checked="" type="checkbox"/>	Alarm system	340/525
17	US 49910 83 A	<input checked="" type="checkbox"/>	Method and system for extending address space for vector processing	711/207
18	US 49263 20 A	<input checked="" type="checkbox"/>	Information processing system having microprogram-controlled type arithmetic processing unit	713/400
19	US 49263 17 A	<input checked="" type="checkbox"/>	Hierarchical memory system with logical cache, physical cache, and address translation unit for generating a sequence of physical addresses	711/3
20	US 49166 95 A	<input checked="" type="checkbox"/>	Stored program controlled real time system including three substantially identical processors	714/11
21	US 48917 87 A	<input checked="" type="checkbox"/>	Parallel processing system with processor array having SIMD/MIMD instruction processing	712/205
22	US 48827 02 A	<input checked="" type="checkbox"/>	Programmable controller with I/O expansion module located in one of I/O module positions for communication with outside I/O modules	710/2

	Docum ent ID	U	Title	Current OR
23	US 48736 26 A	<input checked="" type="checkbox"/>	Parallel processing system with processor array having memory system included in system memory	710/120
24	US 48687 38 A	<input checked="" type="checkbox"/>	Operating system independent virtual memory computer system	710/26
25	US 48477 55 A	<input checked="" type="checkbox"/>	Parallel processing method and apparatus for increasing processing throughput by parallel processing low level instructions having natural concurrencies	712/203
26	US 48377 30 A	<input checked="" type="checkbox"/>	Linking scalar results directly to scalar operation inputs on a bidirectional databus in a computer which superpositions vector and scalar operations	712/7
27	US 48170 91 A	<input checked="" type="checkbox"/>	Fault-tolerant multiprocessor system	714/8
28	US 48169 90 A	<input checked="" type="checkbox"/>	Method and apparatus for fault-tolerant computer system having expandable processor section	709/400
29	US 48129 72 A	<input checked="" type="checkbox"/>	Microcode computer having dispatch and main control stores for storing the first and the remaining microinstructions of machine instructions	712/211
30	US 48071 16 A	<input checked="" type="checkbox"/>	Interprocessor communication	710/113
31	US 47605 18 A	<input checked="" type="checkbox"/>	Bi-directional databus system for supporting superposition of vector and scalar operations in a computer	710/107
32	US 47501 77 A	<input checked="" type="checkbox"/>	Digital data processor apparatus with pipelined fault tolerant bus protocol	714/748
33	US 47018 47 A	<input checked="" type="checkbox"/>	Adaptive instruction sequence synthesizer and process	713/1
34	US 46725 37 A	<input checked="" type="checkbox"/>	Data error detection and device controller failure detection in an input/output system	714/56
35	US 46725 35 A	<input checked="" type="checkbox"/>	Multiprocessor system	710/38
36	US 46548 57 A	<input checked="" type="checkbox"/>	Digital data processor with high reliability	714/5
37	US 46462 45 A	<input checked="" type="checkbox"/>	Modular installation for assembling and/or machining parts, with work stations including keyboard-display devices	700/113
38	US 46398 64 A	<input checked="" type="checkbox"/>	Power interlock system and method for use with multiprocessor systems	714/14
39	US 46213 60 A	<input checked="" type="checkbox"/>	Control method of data transfer	370/438
40	US 46202 75 A	<input checked="" type="checkbox"/>	Computer system	712/6
41	US 45970 84 A	<input checked="" type="checkbox"/>	Computer memory apparatus	714/805
42	US 45831 60 A	<input checked="" type="checkbox"/>	Priority control apparatus for a bus in a bus control system having input/output devices	710/107
43	US 45218 50 A	<input checked="" type="checkbox"/>	Instruction buffer associated with a cache memory unit	712/200
44	US 45190 33 A	<input checked="" type="checkbox"/>	Control state sequencer	711/103
45	US 45190 28 A	<input checked="" type="checkbox"/>	CPU with multi-stage mode register for defining CPU operating environment including charging its communications protocol	713/600

	Docum ent ID	U	Title	Current OR
46	US 45105 65 A	<input checked="" type="checkbox"/>	Programmable controller with intelligent positioning I/O modules	700/7
47	US 45091 16 A	<input checked="" type="checkbox"/>	Special instruction processing unit for data processing system	710/105
48	US 44868 26 A	<input checked="" type="checkbox"/>	Computer peripheral control apparatus	714/9
49	US 44842 75 A	<input checked="" type="checkbox"/>	Multiprocessor system	710/40
50	US 44532 15 A	<input checked="" type="checkbox"/>	Central processing apparatus for fault-tolerant computing	714/11
51	US 44518 82 A	<input checked="" type="checkbox"/>	Data processing system	712/32
52	US 44438 65 A	<input checked="" type="checkbox"/>	Processor module for a programmable controller	712/242
53	US 43957 58 A	<input checked="" type="checkbox"/>	Accelerator processor for a data processing system	712/34
54	US 43815 42 A	<input checked="" type="checkbox"/>	System for interrupt arbitration	710/264
55	US 43731 79 A	<input checked="" type="checkbox"/>	Dynamic address translation system	711/207
56	US 43652 95 A	<input checked="" type="checkbox"/>	Multiprocessor system	711/206
57	US 43565 50 A	<input checked="" type="checkbox"/>	Multiprocessor system	714/14
58	US 43475 63 A	<input checked="" type="checkbox"/>	Industrial control system	700/8
59	US 43397 94 A	<input checked="" type="checkbox"/>	Method and system for controlling input/output in process control	710/52
60	US 43131 60 A	<input checked="" type="checkbox"/>	Distributed input/output controller system	710/23
61	US 42701 84 A	<input checked="" type="checkbox"/>	Microprocessor-based programmable logic controller	712/248
62	US 42570 97 A	<input checked="" type="checkbox"/>	Multiprocessor system with demand assignable program paging stores	711/119
63	US 42297 90 A	<input checked="" type="checkbox"/>	Concurrent task and instruction processor and method	718/101
64	US 42284 96 A	<input type="checkbox"/>	Multiprocessor system	710/100
65	US 41797 36 A	<input type="checkbox"/>	Microprogrammed computer control unit capable of efficiently executing a large repertoire of instructions for a high performance data processing unit	712/232
66	US 41248 89 A	<input type="checkbox"/>	Distributed input/output controller system	710/2
67	US 41248 88 A	<input type="checkbox"/>	Peripheral-unit controller apparatus	710/8
68	US 41139 89 A	<input type="checkbox"/>	Electronic telephone system featuring switching networks having thyristors for single-wire switching	379/257

	Docum ent ID	U	Title	Current OR
69	US 41058 76 A	<input type="checkbox"/>	Electronic telephone system featuring periodic scanning of all peripheral units and polling of specific peripheral units for transmission of status and/or instruction information	379/257
70	US 41058 75 A	<input type="checkbox"/>	Electronic telephone switching system comprising a speech-path switching matrix and tone-connecting matrix and employing electronic crosspoint switching devices	379/16
71	US 41058 74 A	<input type="checkbox"/>	Centrally controlled electronic telephone system having a customer memory for storing information on two or more different subscriber stations and peripheral equipment-specific information	379/257
72	US 41058 73 A	<input type="checkbox"/>	Electronic telephone switching system comprising a speech path switching matrix and tone-connecting switching matrix and employing electronic crosspoint switches	379/257
73	US 41058 72 A	<input type="checkbox"/>	Electronic telephone system including interexchange trunk repeaters for traffic with other systems	379/257
74	US 41058 71 A	<input type="checkbox"/>	Electronic telephone system featuring a customer memory within a central control unit connected by bus lines	379/280
75	US 41006 01 A	<input type="checkbox"/>	Multiplexer for a distributed input/out controller system	710/32
76	US 40992 41 A	<input type="checkbox"/>	Apparatus for facilitating a cooperation between an executive computer and a reserve computer	709/400
77	US 40806 49 A	<input type="checkbox"/>	Balancing the utilization of I/O system processors	710/48
78	US 40457 82 A	<input type="checkbox"/>	Microprogrammed processor system having external memory	710/5
79	US 40443 33 A	<input type="checkbox"/>	Data processing switching system	710/316
80	US 40245 07 A	<input type="checkbox"/>	Arrangement for monitoring the state of memory segments	711/170
81	US 40245 05 A	<input type="checkbox"/>	Interface system for coupling an indeterminate number of peripheral devices to a central processing unit	710/2
82	US 40152 42 A	<input type="checkbox"/>	Device for coupling several data processing units to a single memory	718/103
83	US 39797 28 A	<input type="checkbox"/>	Array processors	712/16
84	US 38738 19 A	<input type="checkbox"/>	Apparatus and method for fault-condition signal processing	714/47
85	US 38368 89 A	<input type="checkbox"/>	PRIORITY INTERRUPTION CIRCUITS FOR DIGITAL COMPUTER SYSTEMS	710/264
86	US 38052 45 A	<input type="checkbox"/>	I/O DEVICE ATTACHMENT FOR A COMPUTER	710/62
87	US 37019 76 A	<input type="checkbox"/>	FLOATING POINT ARITHMETIC UNIT FOR A PARALLEL PROCESSING COMPUTER	708/209
88	US 36465 23 A	<input type="checkbox"/>	COMPUTER	717/143
89	US 36147 40 A	<input type="checkbox"/>	DATA PROCESSING SYSTEM WITH CIRCUITS FOR TRANSFERRING BETWEEN OPERATING ROUTINES, INTERRUPTION ROUTINES AND SUBROUTINES	712/228

	Docum ent ID	U	Title	Current OR
1	JP 11163 087 A	<input type="checkbox"/>	SUBSTRATE PROCESSING DEVICE AND TRANSPORTATION SCHEDULING METHOD	
2	JP 01013 628 A	<input type="checkbox"/>	BRANCH CONDITION DETERMINING DEVICE	
3	JP 54107 235 A	<input type="checkbox"/>	INTERRUPT CONTROL SYSTEM	
4	EP 11825 44 A2	<input type="checkbox"/>	Multiprocessor system with multiple instruction sources	
5	EP 40455 9 A2	<input type="checkbox"/>	Multiprocessor system with multiple instruction sources.	
6	WO 20030 10681 A	<input type="checkbox"/>	System for digital signal processing within an adaptive computing engine has status network for routing status word data resulting from instruction execution in set of composite blocks	
7	WO 20020 8859 A	<input type="checkbox"/>	Code translator for central processing unit of programmable computing system, translates instruction from both sequential and target paths of conditional branch instruction	
8	US 60947 15 A	<input type="checkbox"/>	Array processing system for business applications, includes processing elements which execute single instruction stream independently of fixed time relationship between processing elements	
9	JP 09198 236 A	<input type="checkbox"/>	Instruction sequence decision method for forming source program from flowchart - involves detecting graphic data of functional block linked to next block and stored in second buffer	
10	US 54288 11 A	<input type="checkbox"/>	Interface between register file for arbitrating between single and multiple cycle instruction execution co-processor functional units - asserts execution unit write line, between single and multiple cycle units, when single cycle unit requests access to destination bus, and uses arbitration system in multiple cycle unit to prevent bus access when certain lines are asserted	
11	US 53613 89 A	<input type="checkbox"/>	Emulation routine instruction issue system - issues each host instruction required in emulation of source instruction program to CPU and uses virtual program counter to indicate address of next host instruction to be executed	
12	EP 51950 9 A	<input type="checkbox"/>	Woofer loudspeaker module for use in television set - has enclosure with front and rear passages from woofer to open ends with rear passage having upstream expansion and downstream regions	
13	DE 40103 11 A	<input type="checkbox"/>	Data processor with interrupt control - allows interruption of central processing unit in response to direct memory access command	
14	WO 86030 38 A	<input type="checkbox"/>	Instruction flow computer - includes network which interconnects process control unit with function units and memory units with parallel program execution	
15	GB 21425 07 A	<input type="checkbox"/>	Data transfer controlling method for picture processor - using gate circuit to detect coincidence of data send and accept ready states in two operation modules	

	Docum ent ID	U	Title	Current OR
1	US 20040 05487 2 A1	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
2	US 20040 03995 2 A1	<input checked="" type="checkbox"/>	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/300
3	US 20040 02518 2 A1	<input checked="" type="checkbox"/>	Method, system and computer readable medium for a raido communication processing unit	725/61
4	US 20040 02493 8 A1	<input checked="" type="checkbox"/>	Flexible interrupt handling methods for optical networking apparatuses with multiple multi-protocol optical networking modules	710/260
5	US 20040 01565 4 A1	<input checked="" type="checkbox"/>	Storage subsystem, information processing system and method of controlling I/O interface	711/113
6	US 20030 23163 3 A1	<input checked="" type="checkbox"/>	Router apparatus	370/395 .31
7	US 20030 20053 9 A1	<input checked="" type="checkbox"/>	Function unit based finite state automata data structure, transitions and methods for making the same	717/161
8	US 20030 20037 8 A1	<input checked="" type="checkbox"/>	Providing a register file memory with local addressing in a SIMD parallel processor	711/1
9	US 20030 19619 7 A1	<input checked="" type="checkbox"/>	Methods and systems for integrated scheduling and resource management for a compiler	717/161
10	US 20030 17992 7 A1	<input checked="" type="checkbox"/>	Image processing apparatus and image processing method	382/173
11	US 20030 07911 3 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/205
12	US 20030 07006 0 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
13	US 20030 05613 4 A1	<input checked="" type="checkbox"/>	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/324
14	US 20030 05608 7 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
15	US 20030 05608 6 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
16	US 20030 03117 2 A1	<input checked="" type="checkbox"/>	TCP receiver acceleration	370/389
17	US 20030 02875 0 A1	<input checked="" type="checkbox"/>	Method and system for digital signal processing in an adaptive computing engine	712/10

	Docum ent ID	U	Title	Current OR
18	US 20030 02832 0 A1	<input checked="" type="checkbox"/>	Navigation apparatus	701/210
19	US 20030 00964 3 A1	<input checked="" type="checkbox"/>	Two-stage request protocol for accessing remote memory data in a NUMA data processing system	711/155
20	US 20030 00963 4 A1	<input checked="" type="checkbox"/>	Non-uniform memory access (NUMA) data processing system that provides notification of remote deallocation of shared data	711/141
21	US 20030 00963 2 A1	<input checked="" type="checkbox"/>	Method and system for prefetching utilizing memory initiated prefetch write operations	711/137
22	US 20030 00962 3 A1	<input checked="" type="checkbox"/>	Non-uniform memory access (NUMA) data processing system having remote memory cache incorporated within system memory	711/119
23	US 20020 18147 9 A1	<input checked="" type="checkbox"/>	Protection system, virtual concatenation processing block, node and ring network	370/404
24	US 20020 18139 2 A1	<input checked="" type="checkbox"/>	Protection system, layer 2 function block, node and ring network enabling wideband transmission of working traffic and protection of protection channel traffic	370/216
25	US 20020 16996 9 A1	<input checked="" type="checkbox"/>	Information processing unit having tamper - resistant system	713/190
26	US 20020 15236 6 A1	<input checked="" type="checkbox"/>	Parallel computer with improved access to adjacent processor and memory elements	712/11
27	US 20020 14408 6 A1	<input checked="" type="checkbox"/>	Multiprocessor system, multiprocessor control method, and multiprocessor control program retaining computer-readable recording medium	712/35
28	US 20020 13378 4 A1	<input checked="" type="checkbox"/>	Automatic design of VLIW processors	716/1
29	US 20020 13326 0 A1	<input checked="" type="checkbox"/>	Operating method of vacuum processing system and vacuum processing system	700/121
30	US 20020 13325 7 A1	<input checked="" type="checkbox"/>	Operating method of vacuum processing system and vacuum processing system	700/117
31	US 20020 13325 6 A1	<input checked="" type="checkbox"/>	Operating method of vacuum processing system and vacuum processing system	700/117
32	US 20020 12091 4 A1	<input checked="" type="checkbox"/>	Automatic design of VLIW processors	716/17
33	US 20020 11212 9 A1	<input checked="" type="checkbox"/>	Efficient instruction cache coherency maintenance mechanism for scalable multiprocessor computer system with store-through data cache	711/141
34	US 20020 11212 4 A1	<input checked="" type="checkbox"/>	Efficient instruction cache coherency maintenance mechanism for scalable multiprocessor computer system with write-back data cache	711/122

	Document ID	U	Title	Current OR
35	US 20020 08329 6 A1	<input checked="" type="checkbox"/>	PARALLEL COMPUTER WITH IMPROVED ACCESS TO ADJACENT PROCESSOR AND MEMORY ELEMENTS	712/11
36	US 20020 07828 5 A1	<input checked="" type="checkbox"/>	Reduction of interrupts in remote procedure calls	710/260
37	US 20020 05298 5 A1	<input checked="" type="checkbox"/>	Storage subsystem, information processing system and method of controlling I/O interface	710/5
38	US 20020 04042 8 A1	<input checked="" type="checkbox"/>	Computer system and method of controlling computation	712/225
39	US 20020 03776 9 A1	<input checked="" type="checkbox"/>	Game system, storage medium, and entertainment apparatus	463/31
40	US 20020 03068 7 A1	<input checked="" type="checkbox"/>	Memory access methods in a unified memory system	345/534
41	US 20020 02932 8 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
42	US 20020 01690 3 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
43	US 20020 01681 5 A1	<input checked="" type="checkbox"/>	Web function block in automation equipment	709/203
44	US 20010 03624 2 A1	<input checked="" type="checkbox"/>	In-core fixed nuclear instrumentation system and power distribution monitoring system	376/245
45	US 20010 01873 3 A1	<input checked="" type="checkbox"/>	Array-type processor	712/16
46	US 66842 86 B1	<input checked="" type="checkbox"/>	High-speed block transfer circuit	710/307
47	US 66752 85 B1	<input checked="" type="checkbox"/>	Geometric engine including a computational module without memory contention	712/201
48	US 66751 87 B1	<input checked="" type="checkbox"/>	Pipelined linear array of processor elements for performing matrix computations	708/622
49	US 66717 67 B2	<input checked="" type="checkbox"/>	Storage subsystem, information processing system and method of controlling I/O interface	711/100
50	US 66657 67 B1	<input checked="" type="checkbox"/>	Programmer initiated cache block operations	711/3
51	US 66622 75 B2	<input checked="" type="checkbox"/>	Efficient instruction cache coherency maintenance mechanism for scalable multiprocessor computer system with store-through data cache	711/141
52	US 66512 22 B2	<input checked="" type="checkbox"/>	Automatic design of VLIW processors	716/1
53	US 66474 85 B2	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23

	Docum ent ID	U	Title	Current OR
54	US 66339 59 B2	<input checked="" type="checkbox"/>	Non-uniform memory access (NUMA) data processing system that provides notification of remote deallocation of shared data	711/141
55	US 66293 12 B1	<input checked="" type="checkbox"/>	Programmatic synthesis of a machine description for retargeting a compiler	717/136
56	US 66256 59 B1	<input checked="" type="checkbox"/>	Router switches to old routing table when communication failure caused by current routing table and investigates the cause of the failure	709/239
57	US 66187 77 B1	<input checked="" type="checkbox"/>	Method and apparatus for communicating between multiple functional units in a computer environment	710/120
58	US 66153 22 B2	<input checked="" type="checkbox"/>	Two-stage request protocol for accessing remote memory data in a NUMA data processing system	711/145
59	US 66041 90 B1	<input checked="" type="checkbox"/>	Data address prediction structure and a method for operating the same	712/207
60	US 65811 87 B2	<input checked="" type="checkbox"/>	Automatic design of VLIW processors	716/1
61	US 65747 14 B2	<input checked="" type="checkbox"/>	Efficient instruction cache coherency maintenance mechanism for scalable multiprocessor computer system with write-back data cache	711/141
62	US 65679 34 B1	<input checked="" type="checkbox"/>	Method and apparatus for verifying multiprocessing design in a unit simulation environment	714/33
63	US 65079 47 B1	<input checked="" type="checkbox"/>	Programmatic synthesis of processor element arrays	717/160
64	US 64969 40 B1	<input checked="" type="checkbox"/>	Multiple processor system with standby sparing	714/4
65	US 64907 16 B1	<input checked="" type="checkbox"/>	Automated design of processor instruction units	716/18
66	US 64217 72 B1	<input checked="" type="checkbox"/>	Parallel computer with improved access to adjacent processor and memory elements	712/11
67	US 64080 41 B2	<input checked="" type="checkbox"/>	In-core fixed nuclear instrumentation system and power distribution monitoring system	376/254
68	US 63935 46 B1	<input checked="" type="checkbox"/>	Physical rename register for efficiently storing floating point, integer, condition code, and multimedia values	712/36
69	US 63857 57 B1	<input checked="" type="checkbox"/>	Auto design of VLIW processors	716/1
70	US 63743 33 B1	<input checked="" type="checkbox"/>	Cache coherency protocol in which a load instruction hint bit is employed to indicate deallocation of a modified cache line supplied by intervention	711/145
71	US 63276 41 B1	<input checked="" type="checkbox"/>	Method of implementing a geometry per wedge (GPW) based headerless solution in a disk drive formatter and a computer program product incorporating the same	711/112
72	US 63109 29 B1	<input checked="" type="checkbox"/>	In-core fixed nuclear instrumentation system and power distribution monitoring system	376/245
73	US 62826 30 B1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
74	US 62825 83 B1	<input checked="" type="checkbox"/>	Method and apparatus for memory access in a matrix processor computer	709/400
75	US 62791 01 B1	<input checked="" type="checkbox"/>	Instruction decoder/dispatch	712/215
76	US 62726 19 B1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41

	Docum ent ID	U	Title	Current OR
77	US 62692 79 B1	<input checked="" type="checkbox"/>	Control system	700/121
78	US 62667 63 B1	<input checked="" type="checkbox"/>	Physical rename register for efficiently storing floating point, integer, condition code, and multimedia values	712/36
79	US 62567 20 B1	<input checked="" type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
80	US 62533 13 B1	<input checked="" type="checkbox"/>	Parallel processor system for processing natural concurrencies and method therefor	712/226
81	US 62471 06 B1	<input checked="" type="checkbox"/>	Processor configured to map logical register numbers to physical register numbers using virtual register numbers	711/203
82	US 62470 93 B1	<input checked="" type="checkbox"/>	Data processing apparatus for executing synchronous instructions prior to executing asynchronous instructions	710/263
83	US 62337 02 B1	<input checked="" type="checkbox"/>	Self-checked, lock step processor pairs	714/48
84	US 62302 62 B1	<input checked="" type="checkbox"/>	Processor configured to selectively free physical registers upon retirement of instructions	712/244
85	US 61822 03 B1	<input checked="" type="checkbox"/>	Microprocessor	712/22
86	US 61579 67 A	<input checked="" type="checkbox"/>	Method of data communication flow control in a data processing system using busy/ready commands	710/19
87	US 61516 89 A	<input checked="" type="checkbox"/>	Detecting and isolating errors occurring in data communication in a multiple processor system	714/49
88	US 61483 91 A	<input checked="" type="checkbox"/>	System for simultaneously accessing one or more stack elements by multiple functional units using real stack addresses	712/202
89	US 61346 51 A	<input checked="" type="checkbox"/>	Reorder buffer employed in a microprocessor to store instruction results having a plurality of entries predetermined to correspond to a plurality of functional units	712/215
90	US 61287 23 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
91	US 61226 56 A	<input checked="" type="checkbox"/>	Processor configured to map logical register numbers to physical register numbers using virtual register numbers	718/100
92	US 61192 23 A	<input checked="" type="checkbox"/>	Map unit having rapid misprediction recovery	712/244
93	US 61150 36 A	<input checked="" type="checkbox"/>	Video game/videographics program editing apparatus with program halt and data transfer features	345/723
94	US 61087 63 A	<input checked="" type="checkbox"/>	Simultaneous parity generating/reading circuit for massively parallel processing systems	712/10
95	US 61015 94 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
96	US 60947 15 A	<input checked="" type="checkbox"/>	SIMD/MIMD processing synchronization	712/20
97	US 60921 81 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
98	US 60852 71 A	<input checked="" type="checkbox"/>	System bus arbitrator for facilitating multiple transactions in a computer system	710/113

	Docum ent ID	U	Title	Current OR
99	US 60790 08 A	<input checked="" type="checkbox"/>	Multiple thread multiple data predictive coded parallel processing system and method	712/11
100	US 60790 06 A	<input checked="" type="checkbox"/>	Stride-based data address prediction structure	711/213
101	US 60702 35 A	<input checked="" type="checkbox"/>	Data processing system and method for capturing history buffer data	712/23
102	US 60472 48 A	<input checked="" type="checkbox"/>	Performance-temperature optimization by cooperatively varying the voltage and frequency of a circuit	702/132
103	US 60386 54 A	<input checked="" type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
104	US 60386 53 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
105	US 60386 44 A	<input checked="" type="checkbox"/>	Multiprocessor system with partial broadcast capability of a cache coherent processing request	711/141
106	US 60385 85 A	<input checked="" type="checkbox"/>	Autonomous distributed instruction book control device	718/100
107	US 60322 52 A	<input checked="" type="checkbox"/>	Apparatus and method for efficient loop control in a superscalar microprocessor	712/233
108	US 60147 41 A	<input checked="" type="checkbox"/>	Apparatus and method for predicting an end of a microcode loop	712/233
109	US 59960 83 A	<input checked="" type="checkbox"/>	Microprocessor having software controllable power consumption	713/322
110	US 59745 65 A	<input checked="" type="checkbox"/>	Composite computer system	714/11
111	US 59745 37 A	<input checked="" type="checkbox"/>	Guard bits in a VLIW instruction control routing of operations to functional units allowing two issue slots to specify the same functional unit	712/215
112	US 59681 67 A	<input checked="" type="checkbox"/>	Multi-threaded data processing management system	712/225
113	US 59681 60 A	<input checked="" type="checkbox"/>	Method and apparatus for processing data in multiple modes in accordance with parallelism of program by using cache memory	712/14
114	US 59681 59 A	<input checked="" type="checkbox"/>	Interrupt system with fast response time	710/264
115	US 59665 28 A	<input checked="" type="checkbox"/>	SIMD/MIMD array processor with vector processing	712/222
116	US 59648 35 A	<input checked="" type="checkbox"/>	Storage access validation to data messages using partial storage address data indexed entries containing permissible address range validation for message source	709/216
117	US 59616 29 A	<input checked="" type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
118	US 59535 35 A	<input checked="" type="checkbox"/>	Using intelligent bus bridges with pico-code to service interrupts and improve interrupt response	710/260
119	US 59516 28 A	<input checked="" type="checkbox"/>	Method and system for performing a convolution operation	708/420
120	US 59409 28 A	<input checked="" type="checkbox"/>	Surface maintenance machine with computer controlled operational and maintenance systems	15/319
121	US 59407 85 A	<input checked="" type="checkbox"/>	Performance-temperature optimization by cooperatively varying the voltage and frequency of a circuit	702/132

	Docum ent ID	U	Title	Current OR
122	US 59368 71 A	<input checked="" type="checkbox"/>	Method and system for performing an L.sub.2 norm operation	708/517
123	US 59238 90 A	<input checked="" type="checkbox"/>	Method and apparatus for optimizing the handling of synchronous requests to a coupling facility in a sysplex configuration	712/1
124	US 59207 10 A	<input checked="" type="checkbox"/>	Apparatus and method for modifying status bits in a reorder buffer with a large speculative state	712/216
125	US 59149 53 A	<input checked="" type="checkbox"/>	Network message routing using routing table information and supplemental enable information for deadlock prevention	370/392
126	US 59055 81 A	<input checked="" type="checkbox"/>	Image forming apparatus	358/468
127	US 59037 72 A	<input checked="" type="checkbox"/>	Plural operand buses of intermediate widths coupling to narrower width integer and wider width floating point superscalar processing core	712/33
128	US 58988 65 A	<input checked="" type="checkbox"/>	Apparatus and method for predicting an end of loop for string instructions	712/239
129	US 58812 65 A	<input checked="" type="checkbox"/>	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts	712/218
130	US 58782 41 A	<input checked="" type="checkbox"/>	Partitioning of processing elements in a SIMD/MIMD array processor	712/203
131	US 58706 19 A	<input checked="" type="checkbox"/>	Array processor with asynchronous availability of a next SIMD instruction	712/20
132	US 58705 79 A	<input checked="" type="checkbox"/>	Reorder buffer including a circuit for selecting a designated mask corresponding to an instruction that results in an exception	712/217
133	US 58549 21 A	<input checked="" type="checkbox"/>	Stride-based data address prediction structure	712/239
134	US 58388 94 A	<input checked="" type="checkbox"/>	Logical, fail-functional, dual central processor units formed from three processor units	714/11
135	US 58322 92 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
136	US 58288 60 A	<input checked="" type="checkbox"/>	Data processing device equipped with cache memory and a storage unit for storing data between a main storage or CPU cache memory	712/207
137	US 58288 59 A	<input checked="" type="checkbox"/>	Method and apparatus for setting the status mode of a central processing unit	712/200
138	US 58225 74 A	<input checked="" type="checkbox"/>	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
139	US 58157 15 A	<input checked="" type="checkbox"/>	Method for designing a product having hardware and software components and product therefor	717/141
140	US 58127 57 A	<input checked="" type="checkbox"/>	Processing board, a computer, and a fault recovery method for the computer	714/11
141	US 57940 67 A	<input checked="" type="checkbox"/>	Digital signal processing device	712/35
142	US 57907 76 A	<input checked="" type="checkbox"/>	Apparatus for detecting divergence between a pair of duplexed, synchronized processor elements	714/10
143	US 57846 30 A	<input checked="" type="checkbox"/>	Method and apparatus for processing data in multiple modes in accordance with parallelism of program by using cache memory	712/30
144	US 57685 53 A	<input checked="" type="checkbox"/>	Microprocessor using an instruction field to define DSP instructions	712/208

	Docum ent ID	U	Title	Current OR
145	US 57650 37 A	<input checked="" type="checkbox"/>	System for executing instructions with delayed firing times	713/502
146	US 57650 11 A	<input checked="" type="checkbox"/>	Parallel processing system having a synchronous SIMD processing with processing elements emulating SIMD operation using individual instruction streams	712/20
147	US 57649 38 A	<input checked="" type="checkbox"/>	Resynchronization of a superscalar processor	712/200
148	US 57640 76 A	<input checked="" type="checkbox"/>	Circuit for partially reprogramming an operational programmable logic device	326/38
149	US 57615 23 A	<input checked="" type="checkbox"/>	Parallel processing system having asynchronous SIMD processing and data parallel coding	712/20
150	US 57548 71 A	<input checked="" type="checkbox"/>	Parallel processing system having asynchronous SIMD processing	712/20
151	US 57520 67 A	<input checked="" type="checkbox"/>	Fully scalable parallel processing system having asynchronous SIMD processing	712/16
152	US 57519 55 A	<input checked="" type="checkbox"/>	Method of synchronizing a pair of central processor units for duplex, lock-step operation by copying data into a corresponding locations of another memory	714/12
153	US 57519 32 A	<input checked="" type="checkbox"/>	Fail-fast, fail-functional, fault-tolerant multiprocessor system	714/12
154	US 57517 60 A	<input checked="" type="checkbox"/>	Controller for a telephone system with code screening of incoming calls	379/211 .01
155	US 57485 16 A	<input checked="" type="checkbox"/>	Floating point processing unit with forced arithmetic results	708/497
156	US 57376 29 A	<input checked="" type="checkbox"/>	Dependency checking and forwarding of variable width operands	712/23
157	US 57297 58 A	<input checked="" type="checkbox"/>	SIMD processor operating with a plurality of parallel processing elements in synchronization	712/22
158	US 57179 44 A	<input checked="" type="checkbox"/>	Autonomous SIMD/MIMD processor memory elements	712/20
159	US 57130 37 A	<input checked="" type="checkbox"/>	Slide bus communication functions for SIMD/MIMD array processor	702/33
160	US 57088 36 A	<input checked="" type="checkbox"/>	SIMD/MIMD inter-processor communication	712/20
161	US 57087 95 A	<input checked="" type="checkbox"/>	Asynchronous access system for multiprocessor system and processor module used in the asynchronous access system	711/167
162	US 56995 36 A	<input checked="" type="checkbox"/>	Computer processing system employing dynamic instruction formatting	712/216
163	US 56994 60 A	<input checked="" type="checkbox"/>	Image compression coprocessor with data flow control and multiple processing units	382/307
164	US 56945 84 A	<input checked="" type="checkbox"/>	Information processing system capable of quickly processing a parameter and a command necessary for drawing processing	345/553
165	US 56897 20 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution	712/23
166	US 56896 89 A	<input checked="" type="checkbox"/>	Clock circuits for synchronized processor systems having clock generator circuit with a voltage control oscillator producing a clock signal synchronous with a master clock signal	709/400

	Docum ent ID	U	Title	Current OR
167	US 56824 92 A	<input checked="" type="checkbox"/>	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts	712/214
168	US 56805 34 A	<input checked="" type="checkbox"/>	Video game/videographics program fabricating system and method with superimpose control	345/473
169	US 56805 33 A	<input checked="" type="checkbox"/>	Videographics program/video game fabricating system and method	345/473
170	US 56758 07 A	<input checked="" type="checkbox"/>	Interrupt message delivery identified by storage location of received interrupt data	710/260
171	US 56551 31 A	<input checked="" type="checkbox"/>	SIMD architecture for connection to host processor's bus	712/34
172	US 56492 25 A	<input checked="" type="checkbox"/>	Resynchronization of a superscalar processor	712/23
173	US 56424 79 A	<input checked="" type="checkbox"/>	Trace analysis of data processing	714/45
174	US 55926 09 A	<input checked="" type="checkbox"/>	Video game/videographics program fabricating system and method with unit based program processing	345/473
175	US 55903 52 A	<input checked="" type="checkbox"/>	Dependency checking and forwarding of variable width operands	712/23
176	US 55903 48 A	<input checked="" type="checkbox"/>	Status predictor for combined shifter-rotate/merge unit	712/223
177	US 55749 28 A	<input checked="" type="checkbox"/>	Mixed integer/floating point processor core for a superscalar microprocessor with a plurality of operand buses for transferring operand segments	712/23
178	US 55600 32 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
179	US 55532 76 A	<input checked="" type="checkbox"/>	Self-time processor with dynamic clock generator having plurality of tracking elements for outputting sequencing signals to functional units	713/500
180	US 55532 28 A	<input checked="" type="checkbox"/>	Accelerated interface between processors and hardware adapters	345/501
181	US 55420 57 A	<input checked="" type="checkbox"/>	Method for controlling vector data execution	712/222
182	US 55399 11 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
183	US 55220 58 A	<input checked="" type="checkbox"/>	Distributed shared-memory multiprocessor system with reduced traffic on shared bus	711/145
184	US 54506 03 A	<input checked="" type="checkbox"/>	SIMD architecture with transfer register or value source circuitry connected to bus	712/22
185	US 54427 57 A	<input checked="" type="checkbox"/>	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts	712/218
186	US 54288 11 A	<input checked="" type="checkbox"/>	Interface between a register file which arbitrates between a number of single cycle and multiple cycle functional units	712/23
187	US 54189 70 A	<input checked="" type="checkbox"/>	Parallel processing system with processor array with processing elements addressing associated memories using host supplied address value and base register content	712/20
188	US 54045 41 A	<input checked="" type="checkbox"/>	Operation monitoring and controlling apparatus for computer system	713/324
189	US 53613 89 A	<input checked="" type="checkbox"/>	Apparatus and method for emulation routine instruction issue	703/27

	Docum ent ID	U	Title	Current OR
190	US 53534 28 A	<input checked="" type="checkbox"/>	Information processing apparatus in which a cache memory can be operated in both store-in and store-through modes	711/145
191	US 53218 30 A	<input checked="" type="checkbox"/>	Reset method when adaptor module is faulty and computer system executing same	714/23
192	US 52768 19 A	<input checked="" type="checkbox"/>	Horizontal computer having register multiconnect for operand address generation during execution of iterations of a loop of program code	711/214
193	US 52688 56 A	<input checked="" type="checkbox"/>	Bit serial floating point parallel processing system and method	708/514
194	US 52261 28 A	<input checked="" type="checkbox"/>	Horizontal computer having register multiconnect for execution of a loop with a branch	712/241
195	US 52261 26 A	<input checked="" type="checkbox"/>	Processor having plurality of functional units for orderly retiring outstanding operations based upon its associated tags	712/218
196	US 52028 87 A	<input checked="" type="checkbox"/>	Access control method for shared duplex direct access storage device and computer system therefor	714/8
197	US 51650 23 A	<input checked="" type="checkbox"/>	Parallel processing system with processor array and network communications system for transmitting messages of variable length	710/317
198	US 51290 92 A	<input checked="" type="checkbox"/>	Linear chain of parallel processors and method of using same	712/16
199	US 51215 02 A	<input checked="" type="checkbox"/>	System for selectively communicating instructions from memory locations simultaneously or from the same memory locations sequentially to plurality of processing	712/24
200	US 51214 88 A	<input type="checkbox"/>	Sequence controller of an instruction processing unit for placing said unit in a ready, go, hold, or cancel state	712/229